SOLID-STATE IMAGE PICKUP APPARATUS

BACKGROUND OF THE INVENTION

1. Field of the Invention

5   The present invention relates to a solid-state image

pickup apparatus configured using a solid-state image pickup

device of the frame transfer system.

2. Description of the Prior Art(s)

      Fig. 1 is a top plan view schematically showing a CCD

10   solid-state image pickup device of the frame transfer system,

and Fig. 2 is a timing chart illustrating the operation of the

solid-state image pickup device.

      The solid-state image pickup device of the frame transfer

system comprises a light receiving section 1, a storage

15   section 2, a horizontal transfer section 3, and an output

section 4. The light receiving section 1 comprises a

plurality of shift registers, having a plurality of

consecutive bits in the vertical direction, arranged so as to

be parallel to each other. Each bit of these shift registers

20   forms a light receiving bit. Each light receiving bit

generates and accumulates an information charge corresponding

to an object image. The storage section 2 is formed from a

plurality of shift registers consecutive to each shift

register of the light receiving section 1. Each bit of these

25   shift registers forms a storage bit, and each storage bit

temporarily stores the information charge transferred from the

light receiving section 1. The horizontal transfer section 3

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comprises a single shift register, to which each bit is connected the respective output of the plurality of shift registers of the storage section 2, and receives, then sequentially transfers and outputs in the horizontal

5 direction, one line at a time the information charges of one screen stored in the storage section 2. The output section 4 is formed from an electrically independent capacitor and an amplifier obtaining the change in electric potential of the capacitor, and the information charge that is output from the

10 horizontal transfer section 3 is received at the capacitor one bit at a time and converted to a voltage value and output as image signal YO.

To the light receiving section 1 is applied a frame transfer clock ϕF for transferring at high speed the

15 information charge of the light receiving section 1 to the storage section 2 within the blanking period of a vertical scan in synchronization with a vertical synchronization signal VD. To the storage section 2 is applied a vertical transfer clock ϕV for loading the information charges that are

20 transferred and output from the light receiving section 1 by the frame transfer clock ϕF as well as for transferring the loaded information charges for one screen to the horizontal transfer section 3 one line at a time within the blanking period of a horizontal scan in synchronization with a

25 horizontal synchronization signal HD. Then, to the horizontal transfer section 3 is applied a horizontal transfer clock ϕH for transferring the information charges that are loaded into

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the horizontal transfer section 3 one line at a time in response to the vertical transfer clock ϕV to the sequential output section 4 in synchronization with the horizontal synchronization signal HD. As a result, the information charges generated at the light receiving section 1, after being transferred to the storage section 2 in one-screen units, are transferred and output one line at a time to the output section 4 via the horizontal transfer section 3, and the image signal YO is output in consecutive one-line units.

Furthermore, a substrate clock ϕB, which rises for a predetermined period during the vertical scan period, is applied to the semiconductor substrate that forms the solid-state image pickup device. In response to the rise of the substrate clock ϕB, the frame transfer clock ϕF is clocked at the same period as during frame transfer, and the information charges of the light receiving section 1 are completely discharged to the substrate. Therefore, a period L, from the completion of the discharge operation of information charges by the substrate clock ϕB to the initiation of the transfer operation by the frame transfer clock ϕF, becomes the storage time of the information charges. The image signal YO represents a level that is proportional to the quantity of information charges stored in each light receiving pixel of the light receiving section 1 during the storage time L.

In the case of the solid-state image pickup device of the frame transfer system, the storage performance of the information charge of each light receiving pixel is attributed

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to the capacity of the potential well formed within the substrate by action of the transfer electrode located in the light receiving section 1. The capacity of this potential well is determined, for example, by the width of the transfer electrode and width of the transfer channel, and further the voltage of the pulse driving the transfer electrode.

When the width of the transfer electrode or width of the transfer channel narrows with the increased resolution of the solid-state image pickup device, the capacity of the potential well that is formed decreases and the storage performance of the information charge of each light receiving pixel lowers. Furthermore, when the driving pulse is lowered in voltage in order to reduce the power consumption of the device, the capacity of the potential well that is formed decreases further. Therefore, the dynamic range of the solid-state image pickup device becomes narrow and the image pickup conditions become restricted.

SUMMARY OF THE INVENTION

It is therefore an object of the present invention to extend the dynamic range of the solid-state image pickup device and perform image pickup operations over a wide range.

The present invention comprises a solid-state image pickup device in which a first light receiving pixel is arranged in a plurality of lines in one line units and a second light receiving pixel capable of being driven independently from the first light receiving pixel is arranged

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in at least one line units between first light receiving pixels of the plurality of lines, a drive circuit for driving the first and second light receiving pixels of the solid-state image pickup device and performing accumulation of the

5 information charges at mutually different times between the first light receiving pixel and second light receiving pixel as well as transferring and outputting the information charges accumulated in the first and second light receiving pixels independently of each other, a timing control circuit for

10 respectively setting the storage time of information charges at the first light receiving pixel and the storage time of information charges at the second light receiving pixel of the solid-state image pickup device, and a signal processing circuit for generating an image signal by adding a first

15 output corresponding to the first light receiving pixel and a second output corresponding to the second light receiving pixel of the solid-state image pickup device.

According to the present invention, image signals are generated by adding together the outputs corresponding to two

20 types of light receiving pixels for which the accumulation time of information charges can be set independently. Therefore, for an object of low brightness, a sufficient output can be obtained from a light receiving pixel for which a long accumulation time of information charges has been set,

25 and for an object of high brightness, a wide range of image pickup is possible from a light receiving pixel for which a short accumulation time of information charges has been set.

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BRIEF DESCRIPTION OF THE DRAWINGS

Fig. 1 is a schematic top plan view of a solid-state image pickup device of a frame transfer system.

Fig. 2 is a timing chart illustrating the operation of the solid-state image pickup device of the frame transfer system.

Fig. 3 is a block diagram showing a configuration of the solid-state image pickup device of the present invention.

Fig. 4 is a timing chart illustrating the operation of the solid-state image pickup device of the present invention.

Fig. 5 is a waveform diagram of the image data in an analog representation.

Fig. 6 is a potential diagram showing one example of the operation of the solid-state image pickup device of the present invention.

Fig. 7 is a waveform diagram of the transfer clocks achieving the operation of Fig. 6.

Fig. 8 shows a relationship between quantity of received light and output voltage.

Fig. 9 shows a relationship between signal component and smear component.

Fig. 10 is a potential diagram showing another example of the operation of the solid-state image pickup device of the present invention.

Fig. 11 is a waveform diagram of the transfer clocks achieving the operation of Fig. 10.

DESCRIPTION OF THE PREFERRED EMBODIMENTS

Fig. 3 is a block diagram showing the configuration of the solid-state image pickup device of the present invention and Fig. 4 is a timing chart illustrating the operation

5   thereof.

A solid-state image pickup device 11 is identical to the solid-state image pickup device of the frame transfer system shown in Fig. 1, and comprises the light receiving section 1, the storage section 2, the horizontal transfer section 3, and

10   the output section 4. A drive circuit 12 generates in response to various timing signals and supplies to the solid-state image pickup device 11 the frame transfer clock ϕF, the vertical transfer clock ϕV, the horizontal transfer clock ϕH, and the substrate clock ϕB. The frame transfer clock ϕF is

15   applied to the light receiving section 1, and the transfer electrode is clocked at a timing in accordance to the rise of the substrate clock ϕB and the information charges of the light receiving section 1 are transferred at high speed to the storage section 2 within the blanking period of the vertical

20   scan in synchronization with the vertical synchronization signal VD. The substrate clock ϕB is applied to the semiconductor substrate forming the solid-state image pickup device, is made high for a predetermined period at a timing in accordance to a shutter timing signal ST, and causes the

25   information charges of the light receiving section 1 to be discharged to the substrate by action of the frame transfer clock ϕF. Therefore, to each light receiving pixel of the

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light receiving section 1 are accumulated the information

charges during the period L, from completion of the discharge

operation by the substrate clock ϕB to initiation of the

transfer operation by the frame transfer clock ϕF.

5   The solid-state image pickup device 11 has an arrangement

in the vertical direction of pixels, the number of which is at

least twice the required number of scanning lines. Namely, a

plurality of light receiving pixels arranged vertically

corresponds to one scanning line. These light receiving

10   pixels can be set so that the accumulation times of the

information charges are mutually different, and for these

light receiving pixels, at least two types of accumulation

times are set. Accordingly, the shutter timing signal ST sets

the timing of the shutter operation into multiple steps. The

15   shutter operation in the present embodiment refers to the

discharging of the information charges accumulated in a pixel

and the transferring of the information charges of a

particular pixel to another pixel. For example, pixels are

arranged in the vertical direction, the number of which is

20   twice the number of scanning lines for displaying the

reproduction screen, and the accumulation times of the

information charges are set independently for the odd-numbered

lines and for the even-numbered lines. The following

operation is given for the case where the light receiving

25   pixels, the number of which is twice the number of the

horizontal scanning lines, are arranged in the vertical

direction, and the accumulation times for the information

charges are set with a difference between the light receiving pixels of the odd-numbered lines and the light receiving pixels of the even-numbered lines.

The vertical transfer clock ϕV is applied to the storage section 2, the information charges transferred and output from the light receiving section 1 by the frame transfer clock ϕF are loaded to the storage section 2, and the loaded information charges for one screen are transferred one line at a time to the horizontal transfer section 3 at one half the period of the horizontal synchronization signal HD. The horizontal transfer clock ϕH is then applied to the horizontal transfer section 3, the information charges loaded into the horizontal transfer section 3 are sequentially transferred to the output section 4 at every line in synchronization with the vertical transfer clock ϕV. As a result, the information charges accumulated at each light receiving pixel of the light receiving section 1 during the period L are transferred to the storage section 2 in one-screen units, then transferred and output one line at a time to the output section 4 via the horizontal transfer section 3, and the image signal YO is output in consecutive in one-line units.

A timing control circuit 13 generates and supplies to the drive circuit 12 the horizontal synchronization signal HD and vertical synchronization signal VD on the basis of a reference clock having a fixed period. Furthermore, the shutter timing signal ST, which rises during the vertical scan, is generated and supplied to the drive circuit 12. The shutter timing

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signal ST is a 2-bit signal, for example, and sets the timing

of the shutter operation in two steps. A ratio R of the

substantial accumulation times of the information charges

generated from the delay in shutter operation is supplied to

5   the arithmetic circuit 20 to be described hereinafter. At

this time, a value 1/(R-1) is generated in correspondence to

ratio R of the accumulation times and simultaneously supplied

to the arithmetic circuit 20.

An analog processing circuit 14 executes a sample and

10   hold operation and various types of correction operations for

the image signal Y0 that is input from the solid-state image

pickup device 11 and generates an image signal Y1 conforming

to a predetermined format. For example, to generate the image

signal Y1, the sample and hold operation is performed at the

15   timing for obtaining only the signal level for the image

signal Y0 in which the reset level and signal level repeat in

synchronization with the output operation of the solid-state

image pickup device 11. An A/D converter circuit 15

synchronizes with the sample and hold operation of the analog

20   processing circuit 14 and generates image data D1 representing

information on each light receiving pixel of the solid-state

image pickup device 11. At the solid-state image pickup

device 11, in the case where the accumulation time of the

information charges differs between the light receiving pixel

25   of the odd-numbered lines and the light receiving pixel of the

even-numbered lines, the image data D1 is obtained for two

lines during the horizontal scan period as shown in Fig. 5.

At this time, the level of the image data D1 for two lines
obtained within the same horizontal scan period contains a
difference proportional to the ratio of the accumulation times
of the information charges in each light receiving pixel of
the solid-state image pickup device 11.

A line memory 16 stores the image data D1 for one line
during the first half of each horizontal scan period. The
image data D1 stored in the line memory 16 is read out as the
image data D2 after a delayed timing of half the horizontal
scan period. The line memory 16 is configured, for example,
by arranging in parallel two memory circuits, each having the
capacity for storing one line of image data D1, so as to
alternately perform read and write operations of the image
data D1.

The arithmetic circuit 20, comprising first and second
multipliers 21 and 22, first through third subtracters 23, 24,
and 25, and an adder 26, operates during the period when a
gate pulse GP rises and generates a smear data S and a third
image data D3. The first multiplier 21 multiplies the ratio R
that is input from the timing control circuit 13 with the
first image data D1, and the first subtracter 23 subtracts the
second image data D2 from the multiplication result R·D1 of
the first multiplier 21. The second multiplier 22 multiplies
1/(R-1) that is input from the timing control circuit 13 with
the subtraction result S0 of the first subtracter 23. The
multiplication result of the second multiplier 22 is output as
smear data. The second subtracter 24 subtracts the smear data

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S from the second data D2, and the third subtracter 25

subtracts the smear data S from the first data D1. The adder

26 then adds the subtraction result D2' of the second

subtracter 24 and the subtraction result D1' of the third

5   subtracter 25, and outputs the addition result as the third

image data D3.

Fig. 6 is a potential diagram showing one example of a

method for driving the solid-state image pickup device in the

solid-state image pickup apparatus of the present invention,

10   and Fig. 7 is a timing chart of the transfer clocks achieving

the operation thereof. These figures illustrate the case

where the light receiving pixels, the number of which is twice

the number of scanning lines, are arranged in the vertical

direction in the light receiving section 1 of the solid-state

15   image pickup device 11, and the accumulation times of the

information charges are set with a difference between the

light receiving pixels of the odd-numbered lines and the light

receiving pixels of the even-numbered lines.

In the light receiving section 1 of the solid-state image

20   pickup device 11, a plurality of transfer electrodes are

arranged in correspondence to six phases of transfer clocks $\phi 1$

through $\phi 6$, and with respect to the transfer electrodes of the

six phases, two pixels P1 and P2 are substantially defined.

At the initiation of the first image pickup operation,

25   the second transfer clock $\phi 2$ and the fifth transfer clock $\phi 5$

rise, and the potential levels under the respective transfer

electrodes applied with the transfer clocks $\phi 2$ and $\phi 5$ are

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deeply formed. At this time, the other transfer clocks $\phi1$, $\phi3$, $\phi4$, and $\phi6$ remain low, and the potential levels under the transfer electrodes applied with the transfer clocks $\phi1$, $\phi3$, $\phi4$, and $\phi6$ remain shallow. As a result, at a timing t0 during

5   the first charge accumulation period, potential wells are formed under the transfer electrodes applied with the transfer clocks $\phi2$ and $\phi5$, and at these potential wells are accumulated the information charges generated by photoelectric conversion.

At the elapse of a predetermined period L1 from the
10   initiation of storage of the information charges, the third transfer clock $\phi3$ rises, and in succession, the second transfer clock $\phi2$ falls. At a timing t1 after the second transfer clock $\phi2$ falls, the potential well storing information charges, along with the information charges
15   accumulated in period L1, moves from under the transfer electrode applied with the second transfer clock $\phi2$ to under the transfer electrode applied with the third transfer clock $\phi3$. Furthermore, when the third transfer clock $\phi3$ falls after the fourth transfer clock $\phi4$ rises, the potential well, along
20   with the information charges, moves from under the transfer electrode applied with the third transfer clock $\phi3$ to under the transfer electrode applied with the fourth transfer clock $\phi4$. At this time, the information charges accumulated in period L1 under the transfer electrode applied with the second
25   transfer clock $\phi2$ are combined with the information charges accumulated in the same period L1 under the transfer electrode applied with the fifth transfer clock $\phi5$.

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Then, after the second transfer clock $\phi2$ is raised, the fourth transfer clock $\phi4$ is lowered and the second image pickup operation is initiated. As a result, at a timing t2 during the charge accumulation period, similar to the case for timing t0, potential wells are formed under the transfer electrodes applied with the transfer clocks $\phi2$ and $\phi5$, and at these potential wells are again accumulated the information charges generated by photoelectric conversion. The second image pickup operation continues during period L2.

At the potential well under the transfer electrode applied with the second transfer clock $\phi2$, information charges are hardly stored at the initiation of the second image pickup operation. As a result of this, at the potential well under the transfer electrode applied with the second transfer clock $\phi2$, namely, the first light receiving pixel P1, are stored only the information charges generated during period L2, when the second storage operation is performed. On the other hand, at the potential well under the transfer electrode applied with the fifth transfer clock $\phi5$ are stored the information charges accumulated in two potential wells in period L1, when the first image pickup operation was performed. As a result of this, at the potential well under the transfer electrode applied with the fifth transfer clock $\phi5$, namely, the second light receiving pixel P2, the information charges generated during period L3 continuing from the first image pickup operation to the second image pickup operation are accumulated, and furthermore, the information charges

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generated at the first light receiving pixel P1 during period L1, when the first image pickup operation is performed, are added.

After completion of the above-mentioned first and second image pickup operations, the first through sixth transfer clocks $\phi1$ through $\phi6$ are clocked with a mutual phase difference of $2\pi/3$, and the information charges of the light receiving pixels P1 and P2 are transferred and output while respectively independent. As a result, the output corresponding to the first light receiving pixel P1 and the output corresponding to the second light receiving pixel P2, namely, the levels of image data D1 and D2 processed in the arithmetic circuit 20 show the following relationship in the period when the gate pulse rises:

D1:D2 = L2:(L1+L3)

Since the light receiving pixels P1 and P2 usually have equal storage capacities of information charges, the second light receiving pixel P2 becomes saturated at a small quantity of incident light. For example, as shown in Fig. 8, when the output voltage of the first light receiving pixel P1 reaches the saturation level Vs at a quantity of received light m1, the output voltage of the second light receiving pixel P2 reaches the saturation level Vs at a quantity of received light m2, which is smaller than the quantity of received light m1.

In the above-mentioned arithmetic circuit 20, the following processing is executed for the two types of image

data D1 and D2. It is assumed here that the period L1 for performing the first image pickup operation and the period L2 for performing the second image pickup operation are equal, and the period required for transferring the information

5   charge from the first light receiving pixel P1 to the second light receiving pixel P2 is sufficiently smaller than periods L1 and L2 and can thus be ignored. At this time, the ratio R that is input from the timing control circuit 13 is "3" and 1/(R-1) is "1/2".

10   First, the image data D1 is tripled at the first multiplier 21, and as shown in Fig. 9, the tripled image data 3D1 with a level matching that of the image data D2 is generated. Usually, each image data D1 and D2 contains the proper signal component and the smear component combined by

15   the vertical transfer of information charges so that when the image data D1 is tripled, the smear component besides the signal component is also tripled. Accordingly, at the first subtracter 23, when the image data D2 is subtracted from the tripled image data 3D1, the signal component is canceled out

20   leaving the smear component, thus generating the smear data S0. The smear data S0, which is the result of subtracting the singled smear component from the tripled smear component, actually represents a doubled value. Next, when the smear data S0 is multiplied by 1/2 at the second multiplier 22, the

25   smear data S representing the actual smear component is generated.

At the second and third subtracters 24 and 25, the smear

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data S is respectively subtracted from the image data D1 and

D2, and image data D1' and D2', which become only the signal

components, are generated. The image data D1' and D2' are

added together at the adder 26 where a third image data D3 is

5   output.

The aforementioned third image data D3 is obtained by

combining the two types of image data D1 and D2 having

different light receiving sensitivities, and this

substantially extends the dynamic range of the solid-state

10   image pickup device. For example, as shown in Fig. 8, it is

possible to vary the output voltage according to the quantity

of received light until the quantity of received light reaches

m1. If only the dynamic range is observed here, the first

image data D1 varies over the same range. However, since the

15   first image data D1 drops in light receiving sensitivity at

low brightness, a sufficient output cannot be obtained when

the quantity of received light is low. In the case of the

third image data D3, the dynamic range can be extended while

an output of sufficient level is obtained even at low

20   brightness.

Furthermore, the third image data D3 has a different

output voltage level with respect to the quantity of received

light, namely, a different apparent light receiving

sensitivity, when the quantity of received light is between 0

25   and m2, and when the quantity of received light is between m2

and m1. However, from the fact that high sensitivity results

when the quantity of received light is low and low sensitivity

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results when the quantity of received light is high, any

visual deficiency in the reproduction screen can be eliminated

if the ratio of periods L1 and L2, when the respective image

pickup operations are performed, is optimized and the

5   characteristics of the change in the output voltage with

respect to the quantity of received light is approximated to

the gamma correction curve.

Furthermore, since the smear data S is calculated at

every line, the difference in the smear component in every

10   line generated due to the difference in the transfer distance

is correctly represented. Furthermore, since the timing at

which this smear component is obtained is nearly identical to

the timing at which the smear component is combined into the

actual respective image signals of the odd-numbered lines and

15   even-numbered lines, the influence of deterioration with time

of the object is minimal.

Fig. 10 is a potential diagram showing another example of

a method for driving the solid-state image pickup device in

the solid-state image pickup apparatus of the present

20   invention, and Fig. 11 is a timing chart of the transfer

clocks achieving the operation thereof. These figures,

similar to Fig. 6 and Fig. 7, show the case where the light

receiving pixels, the number of which is twice the number of

scanning lines, are arranged in the vertical direction in the

25   light receiving section 1 of the solid-state image pickup

device 11, and the storage times of information charges are

different between the light receiving pixels of the odd-

numbered lines and the light receiving pixels of the even-
numbered lines.

When the first image pickup operation is initiated, the
fifth transfer clock $\phi 5$ rises, and the potential level under
5   the transfer electrodes applied with the transfer clock $\phi 5$ is
deeply formed. At this time, the other transfer clocks $\phi 1$
through $\phi 4$ and $\phi 6$ remain low, and the potential levels under
the transfer electrodes applied with the transfer clocks $\phi 1$
through $\phi 4$ and $\phi 6$ remain shallow. As a result, at timing t0
10   during the first charge accumulation period, a potential well
is formed under the transfer electrode applied with the fifth
transfer clock $\phi 5$, and at this potential well are accumulated
the information charges generated by photoelectric conversion.

The first image pickup operation completes at the elapse
15   of period L1 from the initiation of accumulation of the
information charges, and the second image pickup operation is
initiated at the rise of the second transfer clock $\phi 2$. At the
initiation of the second image pickup operation, only the
second transfer clock $\phi 2$ rises, and the other transfer clocks
20    $\phi 1$ and $\phi 3$ through $\phi 6$ remain the same as at the first image
pickup operation. At timing t1 after the initiation of the
second image pickup operation, a potential well storing the
information charges is also formed under the transfer
electrode applied with the second transfer clock $\phi 2$. As a
25   result, at timing t2 during the charge storage period, a
potential wells are formed under the respective transfer
electrodes applied with the transfer clocks $\phi 2$ and $\phi 5$, and at

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these potential wells are again accumulated the information

charges generated by photoelectric conversion. The second

image pickup operation continues during the period L2.

At the potential well under the transfer electrode

5   applied with the second transfer clock ϕ2, namely, the first

light receiving pixel P1, are accumulated only the information

charges generated during the period L2, when the second

storage operation is performed. On the other hand, at the

potential well under the transfer electrode applied with the

10   fifth transfer clock ϕ5, namely, the second light receiving

pixel P2, are accumulated the information charges generated

through the period L1, when the first image pickup operation

is performed, and the period L2, when the second image pickup

operation is performed.

15   After the completion of the above-mentioned first and

second image pickup operations, similar to the first

embodiment, the first through sixth transfer clocks ϕ1 through

ϕ6 are clocked with a mutual phase difference of 2π/3, and the

information charges of the light receiving pixels P1 and P2

20   are transferred and output while respectively independent. As

a result, the output corresponding to the first light

receiving pixel P1 and the output corresponding to the second

light receiving pixel P2 show the following relationship:

P1:P2 = L2:(L1+L2)

25   The image signals obtained in the above-mentioned manner,

except for the fact that the ratio of the image signal level

corresponding to the first light receiving pixel P1 to the

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image signal level corresponding to the second light receiving pixel P2 is different, can be handled in the same manner as the first embodiment. Therefore, expansion of the dynamic range of the solid-state image pickup device and detection of the smear component become possible.

It should be noted that while examples were given for the case where all lines of the light receiving pixels arranged in the light receiving section were assigned to the first and second light receiving pixels P1 and P2, two adjacent lines among light receiving pixels arranged with three or more consecutive lines may be assigned to the first and second light receiving pixels P1 and P2. For example, with four lines of light receiving pixels, the first light receiving pixel P1 is assigned to the first line, the second light receiving pixel P2 is assigned to the second line, and the third and fourth lines perform the storage of information charges individually without performing the combination of information charges from the other pixels.

Furthermore, the line memory 16 and the arithmetic circuit 20 may respectively comprise a memory circuit capable of storing image data D1 for a suitable number of lines, and a digital signal processing circuit for repeating the reading and writing of data to the memory circuit along with arithmetic operations.

According to the present invention, two types of image signals can be obtained from one solid-state image pickup device, and by executing arithmetic operations for these image

signals, expansion of the dynamic range and detection of the smear component become possible.

While there has been described what are at present considered to be preferred embodiments of the invention, it will be understood that various modifications may be made thereto, and it is intended that the appended claims cover all such modifications as fall within the true spirit and scope of the invention.